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(54) **IN-SITU STRIP PROCESS FOR POLYSILICON ETCHING IN DEEP SUB-MICRON TECHNOLOGY**

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(52) **U.S. Cl.** **134/1.2**; 438/725
(58) **Field of Search** 134/1.2; 438/725, 438/721, 719, 717, 734, 736, 739, 723, 724; 430/5

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(57) **ABSTRACT**

A new method of patterning the polysilicon layer in the manufacture of an integrated circuit device has been achieved. A polysilicon layer is provided overlying a semiconductor substrate. The polysilicon layer may overlie a gate oxide layer and thereby comprise the polysilicon gate for MOS devices. A hard mask layer is provided overlying the polysilicon layer. A resist layer is provided overlying the hard mask layer. The resist layer is patterned to form a resist mask the exposes a part of the hard mask layer. The polysilicon layer is patterned in a plasma dry etching chamber. First, the resist layer is optionally trimmed by etching. Second, the hard mask layer is etched where exposed by the resist mask to form a hard mask that exposes a part of the polysilicon layer. Third, the resist mask is stripped away. Fourth, polymer residue from the resist mask is cleaned away using a chemistry containing CF_4 gas. Fifth, the polysilicon layer is etched where exposed by the hard mask. After the polysilicon layer is so patterned in the dry plasma etch chamber, the hard mask layer is stripped away to complete the patterning of the polysilicon layer in the manufacture of the integrated circuit device.

19 Claims, 6 Drawing Sheets